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Substitute for Form 1449A/PTO INFORMATION DISCLOSURE STATEMENT BY APPLICANT (use as many sheets as necessary)				Complete If Known	
				Application Number	10/661,130
				Filing Date	9/12/2003
				First Named Inventor	Visokay et al.
				Group Art Unit	2825
Examiner Name	MALSAWMA				
Sheet	1	of	2	Attorney Docket No.	TI-35942

U.S. PATENT DOCUMENTS						
Exam. Initials*	Cite No. ¹	U.S. Patent Document		Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number	Kind Code ² (if known)			
AM	AA	4,628,588		McDavid	12/16/1986	Entire Document
	AB	4,641,417		McDavid	02/10/1987	Entire Document
	AC	4,672,419		McDavid	06/09/1987	Entire Document
	AD	4,954,867		Hosaka	09/04/1990	Entire Document
	AF	5,633,522		Dorleans et al.	05/27/1997	Entire Document
	AG	5,723,893		Yu et al.	03/03/1998	Entire Document
	AH	5,937,315		Xiang et al.	08/10/1999	Entire Document
	AJ	6,376,342	B1	Tseng	04/23/2002	Entire Document
	AK	6,410,967	B1	Hause et al.	06/25/2002	Entire Document
	AL	6,432,817	B1	Bertrand et al.	08/13/2002	Entire Document
	AM	6,602,781	B1	Xiang et al.	08/05/2003	Entire Document
	AN	6,617,624	B2	Powell	09/09/2003	Entire Document

FOREIGN PATENT DOCUMENTS								
Exam. Initials*	Cite No. ¹	Foreign Patent Document			Name of Patentee or Applicant of Cited Doc.	Date of Pub. of Cited Doc. (mm-dd-yyyy)	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	† ⁶
		Office ³	Number ⁴	Kind Code ² (if known)				
	BA							
	BB							
	BF							
	BG							
	BH							

OTHER PRIOR ART - NON PATENT LITERATURE DOCUMENTS			
Exam. Initials*	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	† ²
AM	CA	"An Investigation of Molybdenum Gate for Submicrometer CMOS", ROBERT F. KWASNICK, EDMUND B. KAMINSKY, PAUL A. FRANK, GERHARD A. FRANZ, KENNETH J. POLASKO, RICHARD J. IAIA and THOMAS B. GORDZYA, IEEE Transactions on Electron Devices, Vol. 35, No. 9, September, 1988, pp. 1432-1438.	
AM	CB	"Silicon Processing for the VLSI Era, Volume 2: Process Integration", STANLEY WOLF, Ph.D., Copyright, 1990 by Lattice Press, 7 pgs.	
AM	CC	"Electrical Characteristics of TiB ₂ for ULSI Applications", CHANG SIK CHOI, QINGFENG WANG, CARLTON M. OSBURN, GARY A. RUGGLES and AYAN S. SHAH, IEEE Transactions on Electron Devices, Vol. 39, No. 10, October, 1992, pp. 2341-2345.	
Examiner Signature		<i>AM Malbran</i>	Date Considered 7/28/04

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

US and Foreign Patent Documents: ¹Unique citation designation number. ²See attached Kinds of U.S. Patent Documents. ³Enter Office that issued the document, by the two-letter code (WIPO Standard ST.3). ⁴For Japanese patent documents, the indication of the year of the reign of the Emperor must precede the serial number of the patent document. ⁵Kind of document by the appropriate symbols as indicated on the document under WIPO Standard ST. 16 if possible. ⁶Applicant is to place a check mark here if English language Translation is attached.

Other Prior Art/Non-Patent Literature Documents: ¹Unique citation designation number. ²Applicant is to place a check mark here if English Translation is attached.

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				First Named Inventor	Visokay et al.
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				Examiner Name	MALSAWMA
Sheet	2	of	2	Attorney Docket No.	TI-35942

CD	"FinFET Process Refinements for Improved Mobility and Gate Work Function Engineering", YANG-KYU CHOI, LELAND CHANG, PUSHKAR RANADE, JEONG-SOO LEE, DAEWON HA, SRIRAM BALASUBRAMANIAN, ADITYA AGARWAL, MIKE AMEEN TSU-JAE KING and JEFFREY BOKOR, IEEE, 2002, 4 pgs.
CE	"MO ₂ N/Mo GAFF MOSFETs". MANJIN J. KIM and DALE M. BROWN, IEEE, 1982, 4 pgs.
CF	"Application of MoSi ₂ to the Double-Level Interconnections of i ² L Circuits", YOSHITAKA SASAKI, OSAMU OZAWA and SHUICHI KAMEYAMA, IEEE Transactions on Electron Devices, Vol. ED-27, No. 8, August, 1980, 5 pgs.
CG	"Work Function Controlled Silicide Technology for Submicron CMOS", MASAKAZU KAKUMU and KAZUHIKO HASHIMOTO, No source or date available, 2 pgs.
CH	"Refractory Metal Silicide/N ⁺ Polysilicon in CMOS/SOS", B. C. LEUNG and J.S. MAA, No source or date available, 4 pgs.
CI	"Fabrication of Mo-Gate/Ti-Silicide-Clad-Moat MOS Devices by Use of Multilayer-Glass Depositions", J. M. MCDAVID, IEEE Electron Device Letters, Vol. EDL-5, No. 9, September, 1984, 2 pgs.
CJ	"Lightly Impurity Doped (LD) Mo Silicide Gate Technology", MASAKAZU KAKUMU and JUN'ICHI MATSUNAGA, IEEE, 1985, 4 pgs.

Examiner Signature	<i>S. Malawma</i>	Date Considered	7/28/04
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